REMARKS

Favorable reconsideration and allowance of the claims of the present application are respectfully requested.

Before addressing the specific grounds of rejection raised in the present Office Action, applicants have amended Claim 1 to positively recite a step of selectively performing an ion implant and an activation anneal in the at least one other type of device region *forming at least one of an emitter of a bipolar transistor, a polysilicon gate of a field effect transistor or source/drain regions of said field effect transistor*. Likewise, Claim 17 has been amended to positively recite a step of performing a rapid thermal anneal for an emitter/FET activation process on a wafer or chip having a partially formed polysilicon resistor having a polysilicon layer, *said rapid thermal anneal forming at least one of an emitter of a bipolar transistor, a polysilicon gate of a field effect transistor or source/drain regions of said field effect transistor*.

Support for the above amendments to Claims 1 and 17 is found in paragraph [0036] of the present application. Since the above amendments to Claims 1 and 17 do not introduce any new matter into the application, entry thereof is respectfully requested.

In the present Office Action, Claims 1-7, 9 and 11-16 stand rejected under 35 U.S.C. § 102(b) as allegedly anticipated by U.S. Patent No. 5,656,524 to Eklund, et al. ("Eklund, et al."). Claim 8 stands rejected under 35 U.S.C. § 103 as allegedly unpatentable over the combined disclosures of Eklund, et al. and U.S. Patent No. 6,027,964 to Gardner, et al. Claim 10 stands rejected under 35 U.S.C. § 103 as allegedly unpatentable over the combined disclosures of Eklund, et al. and U.S. Patent No. 6,436,747 to Segawa, et al. ("Segawa, et al."). Claims 17-20 stand rejected under 35

U.S.C. § 102 as allegedly unpatentable over the combined disclosures of Eklund, et al. and Segawa, et al.

With respect to the anticipation rejection, it is axiomatic that anticipation under § 102 requires that the prior art reference disclose each and every element of the claim to which it is applied. In re King, 801 F.2d, 1324, 1326, 231 USPQ 136, 138 (Fed. Cir. 1996). Thus, there must be no differences between the subject matter of the claim and the disclosure of the prior art reference. Stated another way, the reference must contain within its four corners adequate direction to practice the invention as claimed. The corollary of the rule is equally applicable: Absence from the applied reference of any claimed element negates anticipation. Kloster Speedsteel AB v. Crucible Inc., 793 F.2d 1565, 1571, 230 USPQ 81, 84 (Fed. Cir. 1986).

Applicants submit that Claims 1-7, 9 and 11-16 of the present application are not anticipated by the disclosure of Eklund, et al. since the applied reference does not disclose applicants' claimed method recited in amended Claim 1. Specifically, Eklund, et al. do not disclose a method of fabricating a precision polysilicon resistor that includes providing a structure that includes at least one polysilicon resistor device region and at least one other type of device region, said at least one polysilicon resistor device region comprising a polysilicon layer; selectively performing an ion implant and an activation anneal in the at least one other type of device region *forming at least one of an emitter of a bipolar transistor, a polysilicon gate of a field effect transistor or source/drain regions of said field effect transistor*; forming a protective dielectric layer overlying said polysilicon layer in said at least one polysilicon resistor device region; and providing a predetermined resistance value to said polysilicon layer in said at least one polysilicon resistor device region.

Eklund, et al. provide a method of fabricating polysilicon resistors that have minimized parasitic capacitance, which are integrated with a bipolar transistor fabrication process. From the description provided in Eklund, et al., a bipolar transistor is partially formed prior to fabricating the resistor. See Col. 3, line 57-Col. 4, line 23. After partially forming the bipolar transistor, the polysilicon for the resistor as well as the emitter is deposited. After deposition of the polysilicon in the resistor region, that polysilicon layer is implanted and then blocked with a patterned mask. See Col. 4, lines 38-44. The patterned mask is present **during implanting of the emitter**. See Col. 4, lines 44-48. Annealing of the polysilicon emitter in the bipolar region and the polsilicon of the resistor then both takes place. As such, Eklund, et al. does not disclose the claimed method recited in amended Claim 1 wherein the emitter of the bipolar transistor is formed, i.e., ion implanted and annealed, prior to providing the predetermined resistance value to the polysilicon layer in the resistor device region. The predetermined resistance value is achieved in the present invention by ion implantation and annealing. See, for example, Claim 6 and Claim 9.

Applicants observe that since Eklund, et al. disclose a different processing sequence than the methodology recited in amended Claim 1, Claims 1-7, 9 and 11-16 are not anticipated by the disclosure of Eklund, et al.

The foregoing remarks clearly demonstrate that the applied reference does not teach each and every aspect of the claimed invention, as required by King and Kloster Speedsteel; therefore the claims of the present application are not anticipated by the disclosure of Eklund, et al. Applicants respectfully submit that the instant § 102 rejection has been obviated and withdrawal thereof is respectfully requested.

With respect to the various § 103 rejections, applicants submit that the claims of the present invention are not rendered unpatentable by the disclosures of Eklund, et al. and Gardner, et al., or Eklund, et al. and Segawa, et al., since none of the applied references teach or suggest applicants' claimed methods recited in independent Claims 1 and 17.

The primary reference, i.e., Eklund, et al., spurring each of the obviousness rejections is defective for the same reasons as discussed above in connection with the anticipation rejection. Applicants thus incorporate the remarks made above herein by reference. To reiterate: Eklund, et al. does not teach or suggest the processing sequence as recited in amended Claim 1. Specifically, Eklund, et al. do not teach or suggest forming an activated emitter region prior to providing a predetermined resistance value into the polysilicon layer of the resistor device region. In Eklund, et al., the polysilicon layer within the resistor region is implanted followed by implantation of the emitter located in the bipolar device region. Both regions are activated together in the prior art method. Applicants observe that independent Claim 17 is not rendered obvious for the same reasoning as discussed above.

The secondary references of Gardner, et al. and Segawa, et al. do not alleviate the above defects in Eklund, et al. since the applied disclosures of Gardner, et al. and Segawa, et al. do not teach or suggest forming activated devices in the other other device regions prior to providing a predetermined resistance value to the polysilicon layer of the resistor. Applicants observe that Gardner, et al. are directed to a method of making an insulated gated field effect transistor and that the reference was relied upon by the Examiner for disclosing the dopant range recited in Claim 8 of the present application.

There is no disclosure in Gardner, et al. of the claimed methods. Segawa, et al., which are directed to a method of making a metal-oxide semiconductor (MOS) device, was relied upon by the Examiner for disclosing the RTA conditions recited in Claim 10 of the present application. There is no disclosure in Segawa, et al. of the claimed methods.

The various § 103 rejections also fail because there is no motivation in the applied references which suggest modifying the disclosed methods to include the processing sequence recited in the claims of the present invention. Thus, there is no motivation provided in the applied references, or otherwise of record, to make the modification mentioned above. "The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." In re Vaeck, 947 F.2d, 488, 493, 20 USPQ 2d. 1438, 1442 (Fed.Cir. 1991).

The rejections under 35 U.S.C. § 103 have been obviated; therefore reconsideration and withdrawal thereof is respectfully requested.

Thus, in view of the foregoing amendments and remarks, it is firmly believed that the present case is in condition for allowance, which action is earnestly solicited.

Respectfully submitted,

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